AGENT :
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IN8089

PMBUS compliant digital power supervisor / MCU

Contents

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1 Overview

1.1 Features

PMBus serial interface:

Query IN/OUT voltage, IN/OUT current, warnings, and faults

Query temperature for up to two temperature sensors

Configure and measure RPM for up to two fans

Configure and driver PWM or 10 bits DAC for up to two fans

Configurable 7-channel 12bits A/D with calibration factors

I2C device-address pin stripping Compatible with most analog controllers Power-on reset

Thermal sense capabilities

UART Communications

MCU (High Performance 8051 μC Core), Instruction set compatible with standard 8051

Memory

- 64K bytes program FLASH with In-System Programming (ISP) capability
- 1024 bytes auxiliary RAM + 256 bytes internal RAM

Peripherals

- 11 general-purpose I/O ports (GPIO),
- Configurable I/O with quasi-bi-directional, input, push-pull, and open-drain modes
- 5 V tolerant when I/O pin define as input pin
- Full-duplex serial port (UART)
- I2C-bus up to 400 kHz, PMBUS up to 100KHz
- Master/Slave Serial Peripheral Interface (SPI)
- Programmable Watchdog Timer (WDT)

Power-On Reset (POR)

Low Voltage Detection (LVD)

Oscillation Options

- Internal oscillator: 12 MHz ± 3% or External oscillator Crystal (33MHz max) or external clock input

Power Saving Modes : Idle Mode or Power-down Mode

Reset Sources

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- Power-On Reset (POR) and Low Voltage Reset (LVR) and External Reset and Watchdog Timer Reset

JTAG Interface :

- On-chip Debug Interface and Programming of Flash and Fuse Bytes through the JTAG Interface

Operating Range

Operating Voltage: 2.4 V to 3.6 V

Operating Temperature: -40 ℃ to +85 ℃

Reliability

8 KV ESD, 4 KV EFT

Package

64-Pin LQFP

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1.2 Description

The IN8089 is a Power Management BUS (PMBUS) protocol compliant, digital power supervisor or MCU, configurable through a host system to meet dynamic converter performance for a multitude of power supply applications.

It is not only to manage power supply operating conditions but also to monitor and report the status back to a host system using the PMBUS protocol.

There are several interfaces

1. PMBus two lines consisting of a serial clock and data, conforming to SMBus V. 2.0, including digital lines called control and one SMAlert.
2. Seven channels of 12-bit resolution A/D for measurement of voltage and current and temperatures and user definable A/D .
3. Two channels of low frequency counters for fan speed measurement. and Pulse Width Modulation (PWM) output or direct DAC for setting a DC level to adjust analog PWM controllers and hence the power supply output voltage.
4. Two channels of temperature measurement, one for local temperature use transistor 2N3906 as sensor and one for external temperature.
5. 11 general-purpose I/O ports (GPIO), user definable.

The IN8089 is also an micro-controller which is instruction-set compatible with the standard 80C51.

There is 64K bytes FLASH memory embedded for user application program. The FLASH can be program by both parallel programming and serial In-System Programming (ISP) with flash memory lock function for code security.

The device also contains 1280 bytes of internal RAM; 11 general-purpose I/O ports; full-duplex serial port (UART), master/slave Serial Peripheral Interface (SPI); 12-bit 7-channel A/D converter for Voltage & Current; & Temperature; Watchdog timer and internal precision oscillator.

1.3 Application

PMBus compliant low voltage, high current density applications

DC power distributed systems

Server Power

Servers and server accessories Telecommunication systems Industrial

ATE power applications Storage systems

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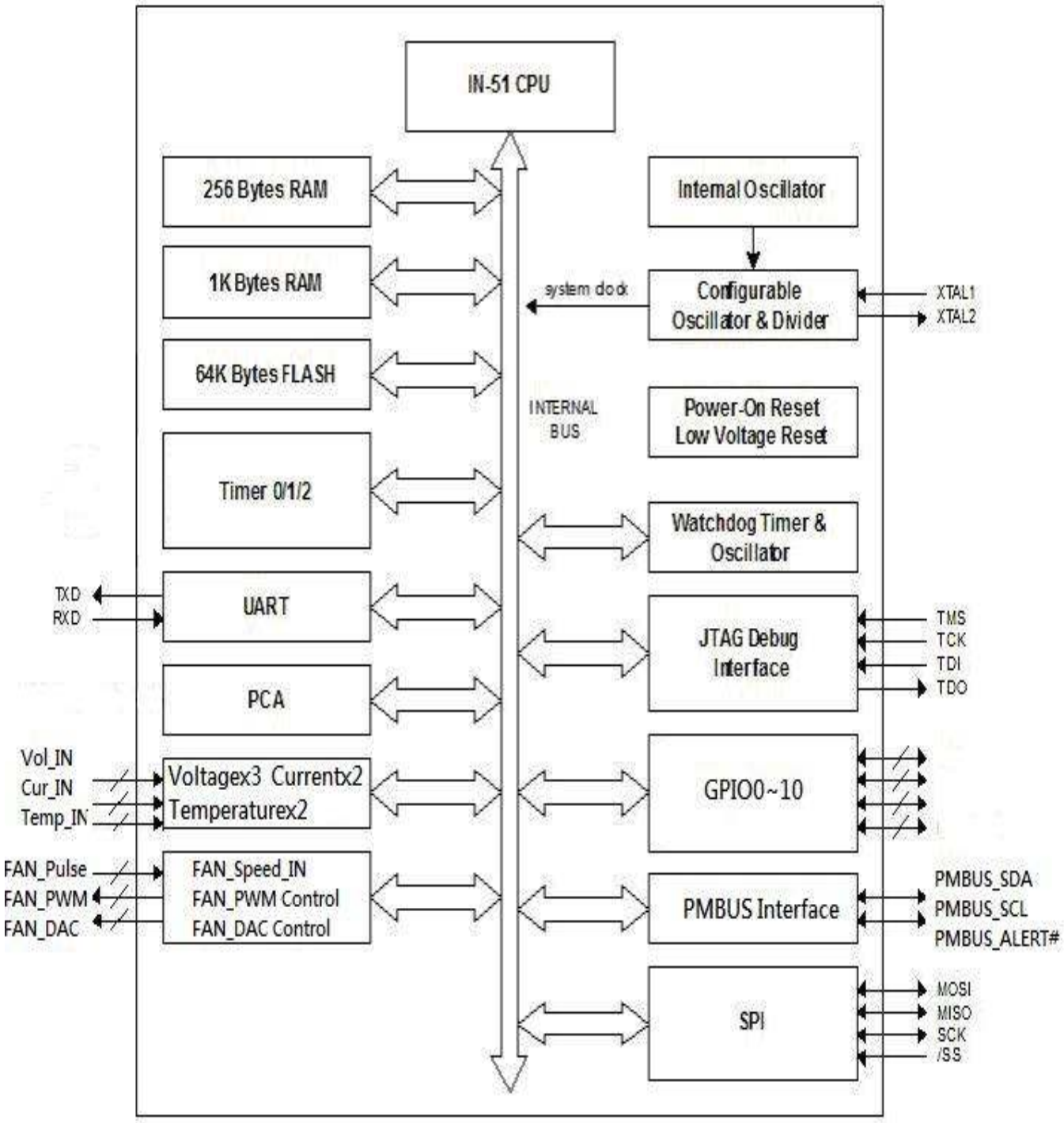
1.4 Block Diagram

Figure 1.1 IN8089 Block Diagram



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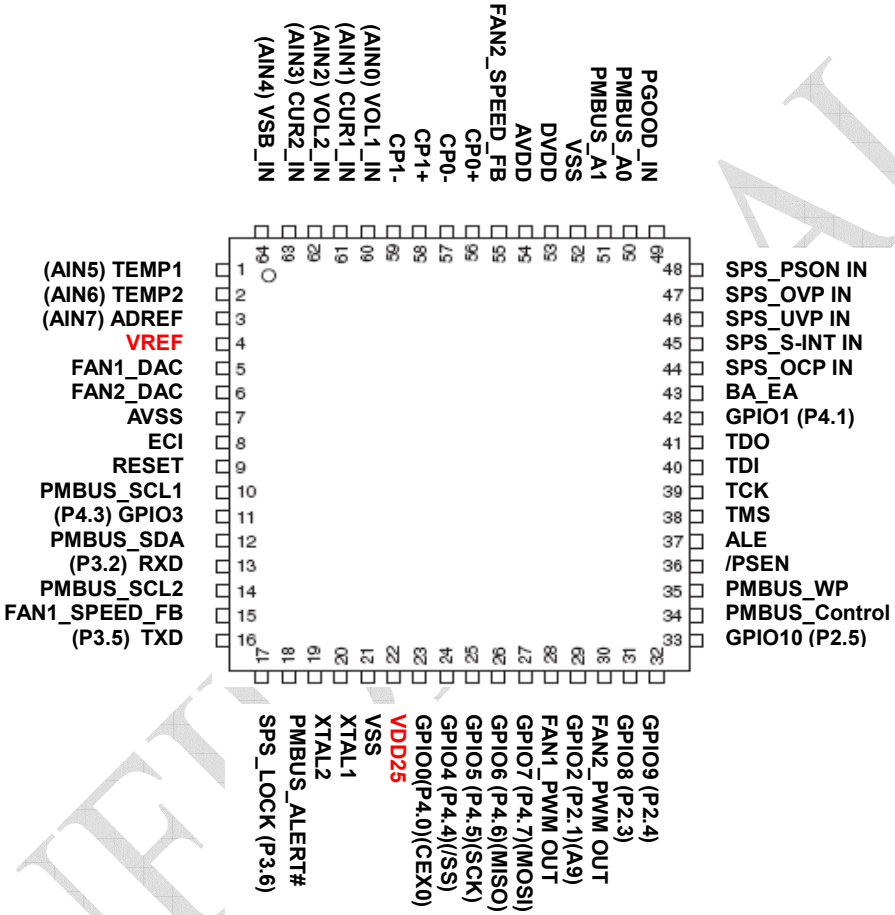
IN8089

1.5 Pin Assignment

LQFP64



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1.6 Pin Description

Table 1-6 Pin Description

Pin Name	Type *	Description
BA_EA	I H	External Access Enable: It must be strapped to VSS in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. It should be strapped to VDD for internal program executions.
/PSEN	O (I H)	Program Store Enable: /PSEN is the read strobe to external program memory. When the MCU is executing code from external program memory, /PSEN is activated twice each 12 clock cycles, except that two /PSEN activations are skipped during each access to external data memory.
ALE	O (I H)	Address Latch Enable: ALE output pulse for latching the low byte of the address during accesses to external memory. In normal operation ALE is emitted at a constant rate of 1/6 the system clock frequency, and may be used for external timing or clocking purposes.
RESET	I (I L)	Reset input. A high level on this pin for longer than minimum pulse length will generate a reset.
XTAL1	I	Crystal oscillator input.
XTAL2	O	Crystal oscillator output.
VSS	I	Ground: Ground potential.
VDD	I	Power Supply: Supply voltage for operation.
VDD25	A O	Internal 2.5 V reference voltage output.
PMBUS_A1	DI	PMBUS Address A1
PMBUS_A0	DI	PMBUS Address A0
SPS_PGOOD IN	DI	Power GOOD signal in
SPS_PSON IN	DI	Power Supply ON signal in
SPS_OVP IN	DI	Over Voltage signal in
SPS_UVP IN	DI	Under Voltage signal in
SPS_S-INT IN	DI	Power system fault interrupt signal in
SPS_OCP IN	DI	Over Current signal in
VOL1_IN (AIN0)	AI	Voltage 1 Converter

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CUR1_IN (AIN1)	AI	Current 1 Converter
VOL2_IN (AIN2)	AI	Voltage 2 Converter
CUR2_IN (AIN3)	AI	Current 2 Converter
VSB_IN (AIN4)	AI	VSB Voltage Converter
TEMP1 (AIN5)	AI	External Temperature sensor Converter
TEMP2 (AIN6)	AI	Local Temperature sensor (use 2N3906) Converter
ADREF (AIN7)	AI	System used, connector to VREF(pin4)
FAN1_PWM OUT	DO	FAN1 PWM Output
FAN2_PWM OUT	DO	FAN2 PWM Output
PMBUS_WP	DI	PMBUS Write data Protect
PMBUS_Control	DI/O	PMBUS CONTROL
GPIO2 (P2.1) GPIO8 (P2.3) GPIO9 (P2.4) GPIO10 (P2.5)	I/O	Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. When 1's are written to Port 2 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that uses 16-bit addresses (MOVX @DPTR). During accesses to external data memory that uses 8-bit addresses (MOVX @RI), Port 2 emits the contents of the P2 Special Function Register.
PMBUS_SCL1	D I/O	PMBUS SCL1 (IIC_HSCL)
PMBUS_SDA	D I/O	PMBUS SDA (IIC-HSDA)
RXD (P3.2)	DI	UART RXD
PMBUS_SCL2	D I/O	PMBUS SCL2, system used, connector to PMBUS_SCL1(pin10)
FAN1_SPEED_FB	DI	FAN1 speed pulse signal in
TXD (P3.5)	DO	UART TXD
LOCK (P3.6)	DI	SPS_LOCK signal in
PMBUS_ALERT#	D I/O	PMBUS_Alert# (SMBAlert#)
GPIO0 (P4.0) GPIO3 (P4.3) GPIO4 (P4.4) GPIO5 (P4.5) GPIO6 (P4.6) GPIO7 (P4.7)	I/O	Port 4 is an 8-bit bi-directional I/O port with internal pull-ups. When 1's are written to Port 4 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 4 pins that are externally being pulled low will source current because of the pull-ups. The output latch corresponding to a secondary function must be programmed to one for that function to operate. The alternative functions are assigned to the pins of port 4 as follows: P4.0(CEX0) : PCA module 0 input/PWM output.

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		P4.3(CEX3) : PCA module 3 input/PWM output. P4.4(/SS) : SPI Slave Select output. P4.5(SCK) : Serial Clock of SPI controller. P4.6(MISO) : Master Input Slave Output of SPI controller. P4.7(MOSI) : Master Output Slave Input of SPI controller.
ECI	I L	PCA external clock input
CP0+, CP0-, CP1+, CP1-	A I	CP0+ : Comparator 0 Non-Inverting Input. CP0- : Comparator 0 Inverting Input. CP1+ : Comparator 1 Non-Inverting Input. CP1- : Comparator 1 Inverting Input.
FAN1_DAC (DAC0)	AO	0~3.3V DAC control FAN1 speed ; DAC0 : DAC 0 Voltage Output.
FAN1_DAC (DAC0)	AO	0~3.3V DAC control FAN2 speed ; DAC1 : DAC 1 Voltage Output
VREF	A O	Internal reference voltage output, 1.275 V ± 0.8 %.
AVDD		Analog supply voltage.
AVSS		Analog ground.
TMS	I H	JTAG Test Mode Select with internal pull-up.
TCK	I H	JTAG Test Clock with internal pull-up.
TDI	I H	JTAG Test Data Input with internal pull-up. TDI is latched on the rising edge of TCK.
TDO	O H	JTAG Test Data Output with internal pull-up. Data is shifted out on TDO on the falling edge of TCK. TDO output is a tri-state driver.

Note: Type **I**: input,

O: output,

I/O: bi-directional,

H: pull-high,

L: pull-low,

D: open drain,

A : analog

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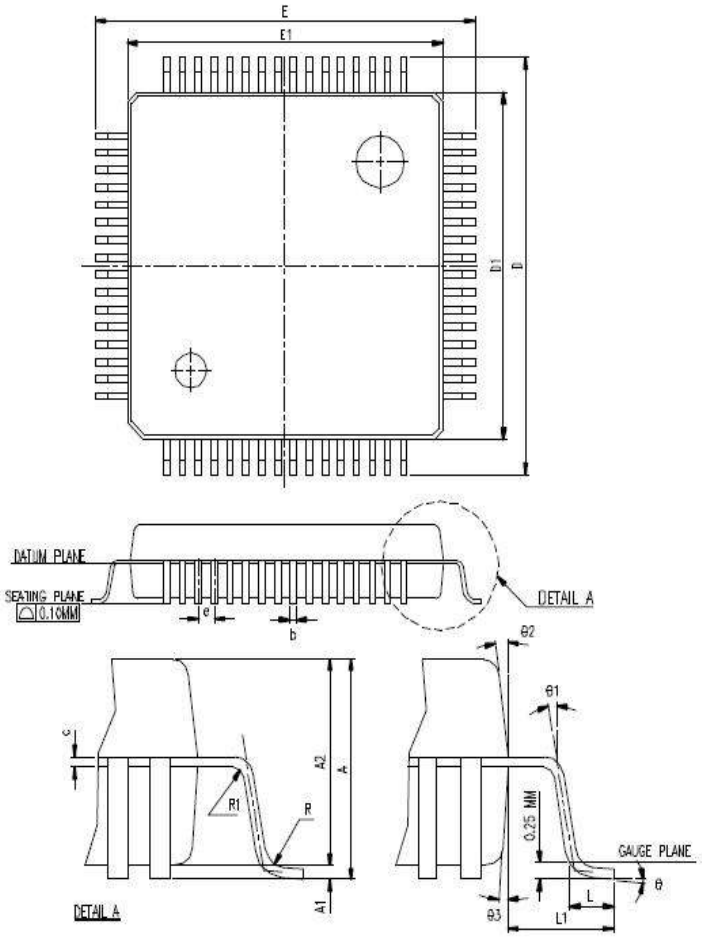
1.7 Package Outline



REV.	DESCRIPTION	BY	DATE
ORIG.	DRAWING ISSUE	SANDY CHEN	98.11.26
A.	ADD NOTES	SANDY CHEN	00.01.21

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09		0.16	0.004		0.006
e	0.50 BASIC			0.020 BASIC		
D	12.00 BASIC			0.472 BASIC		
D1	10.00 BASIC			0.394 BASIC		
E	12.00 BASIC			0.472 BASIC		
E1	10.00 BASIC			0.394 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC	MS-026 (BCD)					

⚠ NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSIN IS 0.25 mm PER SIDE.
" D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

CWT Chant World Technology Inc.			ANGULAR ± 1°
TITLE LQFP 64L PACKAGE OUTLINE BODY SIZE : 10 x 10 MM			ROUGHNESS
			SCALE
DESIGNED Jason Chang 98.11.26		UNIT	QTY
CHECKED C.C. CHO 00.01.26		FILE NAME : P8R064P1	A3
APPROVED C.C. CHO 00.01.26		DWG. NO.:CW-P8-0066	