AGENT：
ATBEL TECHNOLOGY CORP.
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Mixed Signal MCU with
64K Bytes Flash Embedded

1. Features

High Performance 8051 µC Core

Instruction set compatible with standard 8051

High performance processor architecture that executes instructions in one to eight clocks, speed up to 33 MHz

Memory

64/4K bytes of program flash with In-System Programming (ISP) capability

0/60K bytes of program flash with In-Application Programming (IAP) and ISP capability

1280 bytes of data RAM

- 256 bytes internal RAM
- 1K bytes auxiliary RAM (AUXRAM)

Flash memory with security protection

Hardware In-System Programming (ISP) without boot code

Digital Peripherals

Five 8-bit I/O ports

Three 16-bit timers/counters

Full-duplex serial port (UART)

Single Master and Slave I2C interface for external device communication

4-channel Programmable Counter Array (PCA) with PWM, Capture and Compare functions

Master/Slave Serial Peripheral Interface (SPI)

Two external interrupts

6-vector interrupts structure with 2 levels of priority

Programmable Watchdog Timer (WDT)

Analog Peripherals

10-bit, 8-channel, 100 Ksps A/D Converter

Two 10-bit D/A Converters

Two analog comparators

Internal precision reference voltage: 1.275 V ± 0.8 %

Power-On Reset (POR)

Low Voltage Detection (LVD)

Oscillation Options

Internal precision oscillator: 12 MHz ± 3%

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External oscillator: Crystal or external clock input

System clock divider

Power Saving Modes

Idle Mode

Power-down Mode

Reset Sources

Power-On Reset (POR)

Low Voltage Reset (LVR)

External Reset

Watchdog Timer Reset

JTAG Reset

JTAG Interface

On-chip Debug Interface

Programming of Flash and Fuse Bytes through the JTAG Interface

Reliability

8 KV ESD

4 KV EFT

Class-B (30dB) EMI

Operating Range

Operating Voltage: 2.4 V to 3.6 V

Operating Temperature: -40 ℃to +85 ℃

Packages

40-Pin PDIP

44-Pin PLCC

44-Pin LQFP

64-Pin LQFP

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2. Description

The IN6053 is an 8-bit microcontroller which is instruction-set compatible with the standard 80C51 series microcontroller.

There is 64K bytes flash memory embedded for application program. The flash can be program by both parallel programming and Serial In-System Programming (ISP) with flash memory lock function for code security.

The device also contains 256 bytes of internal RAM; 1K bytes of Auxiliary RAM; five 8-bit bi-directional I/O ports; three 16-bit timers/counters; full-duplex serial port (UART), Master/Slave I2C bus interface; 4-channel Programmable Counter Array (PCA); master/slave Serial Peripheral Interface (SPI); internal reference voltage; 10-bit 8-channel A/D converter; two 10-bit D/A converters; two analog comparators; Watchdog timer and internal precision oscillator.

These peripherals are all supported by 6-vector interrupt structure with 2 levels of priority.

The device has two power-reduction modes: Idle mode and Power-down mode, both of which are software selectable. Idle mode turns off the processor clock but allows peripherals to continue operating, while Power-down mode stops the system oscillator for minimum power consumption.

The device also includes JTAG interface can be used for On-chip debugging and Programming for Flash and Fuse bytes.

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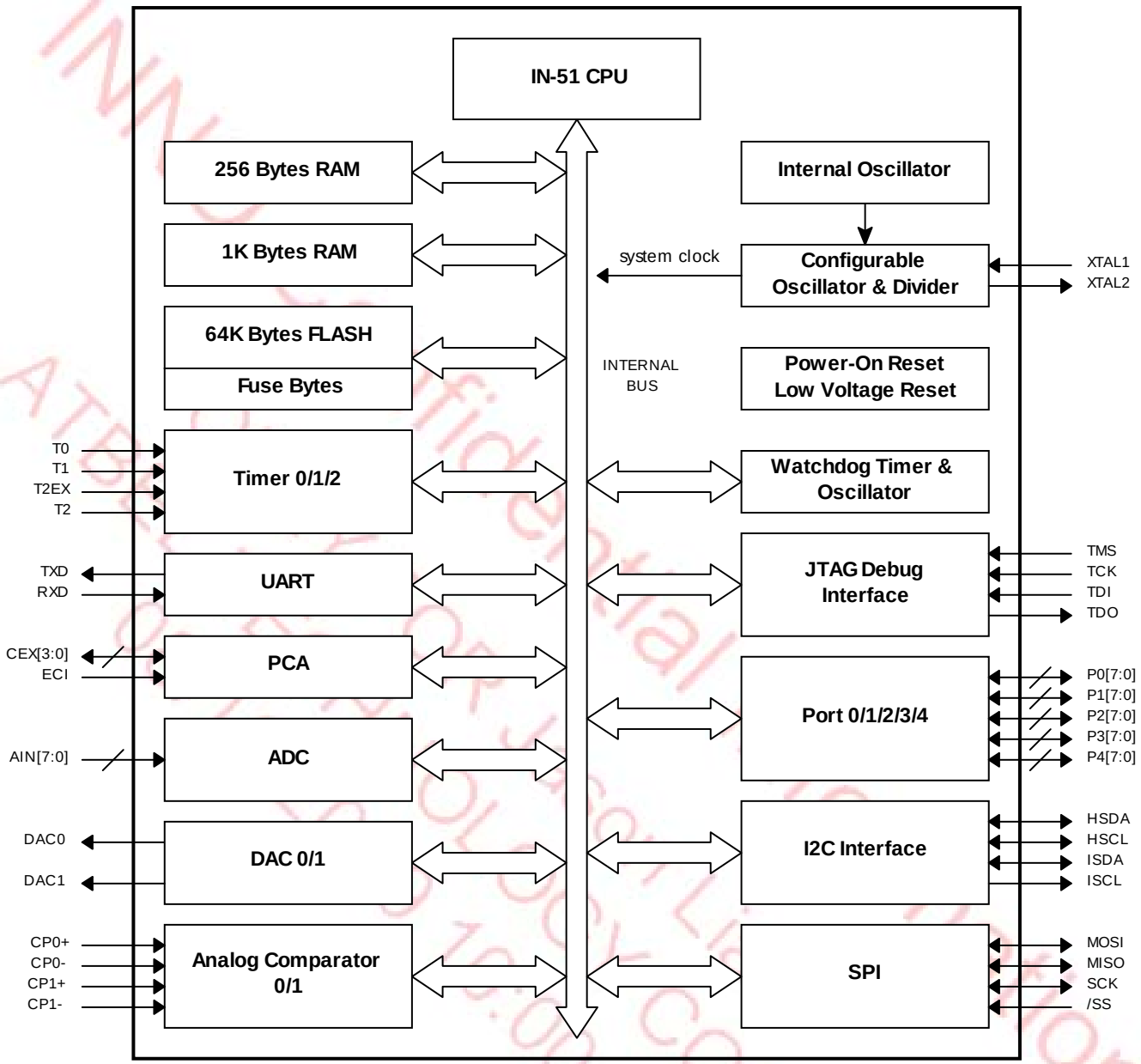
3. Block Diagram

Figure 1. Block Diagram



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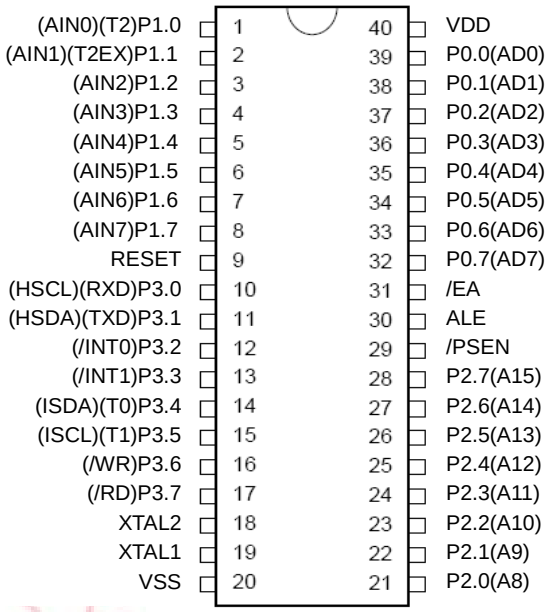
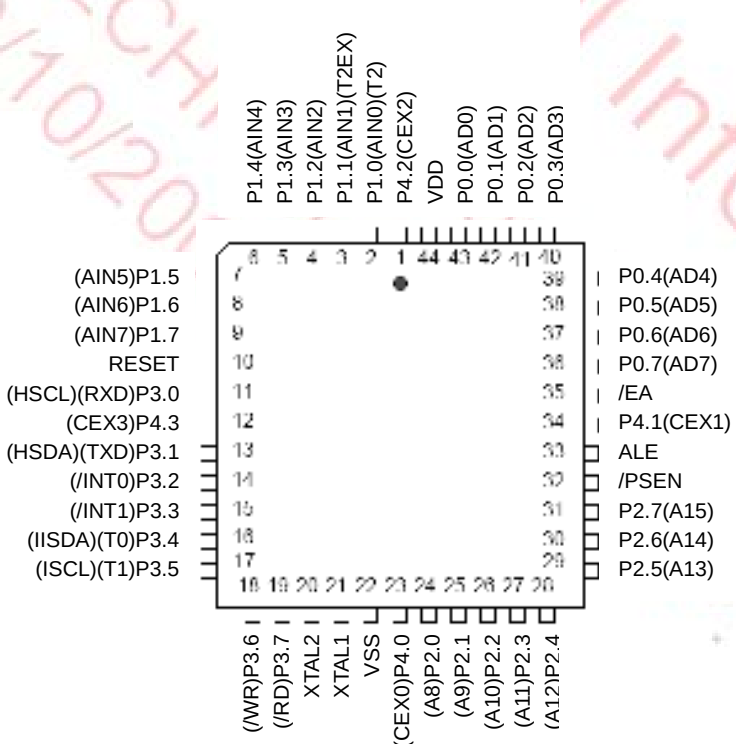
4. Pin Configuration

40-Pin PDIP



44-Pin PLCC



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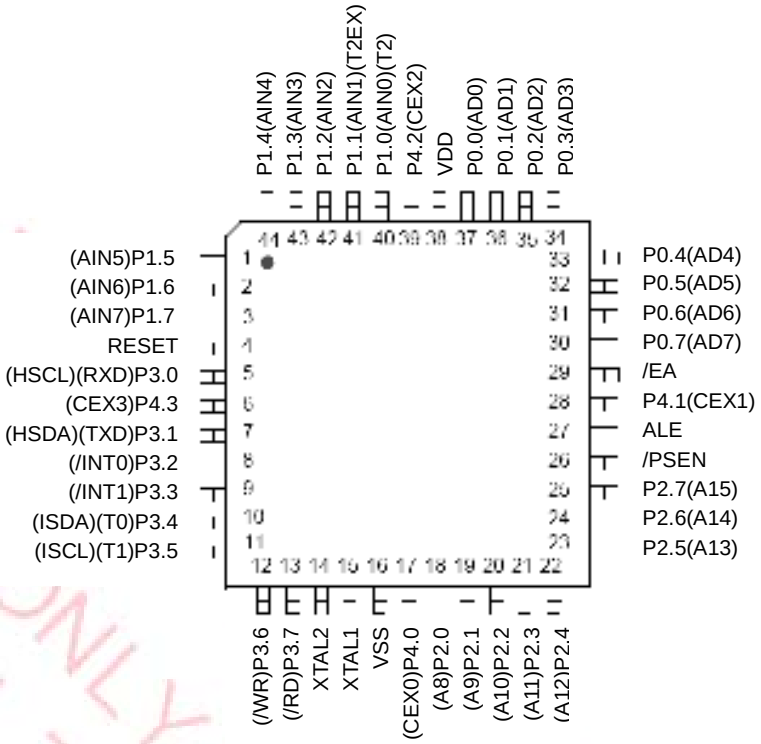
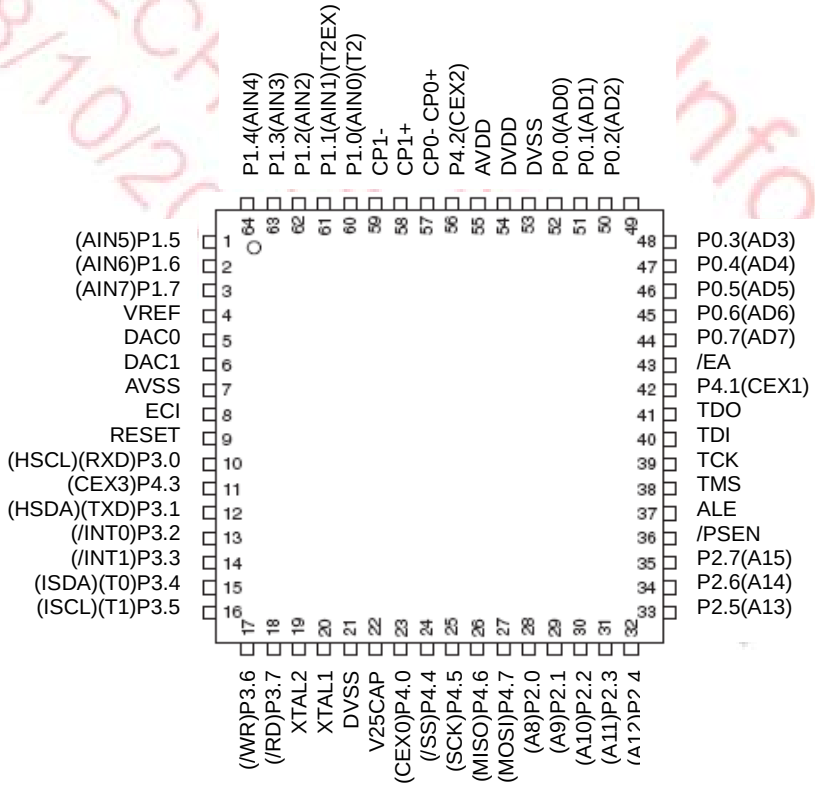
44-Pin LQFP



64-Pin LQFP



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5. Pin Description

Pin Name	Type*	Description
/EA	I H	External Access Enable: /EA must be strapped to logic low in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. /EA should be strapped to logic high for internal program executions.
/PSEN	O (I H)	Program Store Enable: /PSEN is the read strobe to external program memory. When the MCU is executing code from external program memory, /PSEN is activated twice each 12 clock cycles, except that two /PSEN activations are skipped during each access to external data memory.
ALE	O (I H)	Address Latch Enable: ALE output pulse for latching the low byte of the address during accesses to external memory. In normal operation ALE is emitted at a constant rate of 1/6 the system clock frequency, and may be used for external timing or clocking purposes.
RESET	S L	Reset input. A high level on this pin for longer than minimum pulse length will generate a reset.
XTAL1	I	Crystal oscillator input.
XTAL2	O	Crystal oscillator output.
VDD VSS	-	Device supply voltage. Ground.
DVDD DVSS	-	Device digital supply voltage. Digital ground.
AVDD AVSS	-	Device analog supply voltage. Analog ground.
V25CAP	A O	2.5 V regulator output. Connect a 0.1uF capacitor to V25CAP and DVSS.
VREF	A O	Internal reference voltage output, 1.275 V ± 0.8 %.
TMS	I H	JTAG Test Mode Select with internal pull-up.
TCK	I H	JTAG Test Clock with internal pull-up.
TDI	I H	JTAG Test Data Input with internal pull-up. TDI is latched on the rising edge of TCK.
TDO	O H	JTAG Test Data Output with internal pull-up. Data is shifted out on TDO on the falling edge of TCK. TDO output is a tri-state driver.

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P0[7:0]	I/O	Port 0 is an 8-bit open-drain bi-directional I/O port. When 1's are written to port 0 pins, the pins can be used as high-impedance inputs. Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming,
P1[7:0]	I/O H A I	Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. Port 1 pins can be used for digital input/output or as analog inputs for the Analog Digital Converter (ADC). Port 1 pins that have 1's written to them are pulled high by the internal pull-up transistors and can be used as inputs in this state. As inputs, Port 1 pins that are being pulled low externally will be the source of current because of the internal pull-ups. As a secondary digital function, port 1 contains the Timer 2 external trigger/direction control and clock input/output. Port 1 pins are assigned to be used as ADC inputs via the P1C register. The alternative functions are assigned to the pins of port 1 as follows: P1.0(T2)(AIN0) External clock input for Timer/Counter 2 and clock out, ADC input channel 0. P1.1(T2EX)(AIN1) Trigger input for Timer/Counter 2 and direction control, ADC Input channel 1. P1.2(AIN2) ADC Input channel 2. P1.3(AIN3) ADC Input channel 3. P1.4(AIN4) ADC Input channel 4. P1.5(AIN5) ADC Input channel 5. P1.6(AIN6) ADC Input channel 6. P1.7(AIN7) ADC Input channel 7.
P2[7:0]	I/O H	Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. When 1's are written to Port 2 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from

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		external program memory and during accesses to external data memory that uses 16-bit addresses (MOVX @DPTR). During accesses to external data memory that uses 8-bit addresses (MOVX @RI), Port 2 emits the contents of the P2 Special Function Register.
P3[7:0]	I/O H	Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. When 1's are written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current because of the pull-ups. The output latch corresponding to a secondary/third function must be programmed to one for that function to operate. The alternative functions are assigned to the pins of port 3 as follows: P3.0(RXD)(HSCL) Receiver data input of the serial interface, Master/Slave I2C clock. P3.1(TXD) (HSDA) Transmitter data output of the serial interface, Master/Slave I2C data. P3.2(/INT0) External interrupt 0 input/timer 0 gate control input, P3.3(/INT1) External interrupt 1 input/timer 1 gate control input. P3.4(T0)(ISDA) Timer 0 counter input, Master I2C data. P3.5(T1)(ISCL) Timer 1 counter input, Master I2C clock. P3.6(/WR) External data memory write strobe; latches the data byte from port 0 into the external data memory. P3.7(/RD) External data memory read strobe; Enables the external data memory.
P4[7:0]	I/O H	Port 4 is an 8-bit bi-directional I/O port with internal pull-ups. When 1's are written to Port 4 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 4 pins that are externally being pulled low will source current because of the pull-ups.

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		The output latch corresponding to a secondary function must be programmed to one for that function to operate. The alternative functions are assigned to the pins of port 4 as follows: P4.0(CEX0) PCA module 0 input/PWM output. P4.1(CEX1) PCA module 1 input/PWM output. P4.2(CEX2) PCA module 2 input/PWM output. P4.3(CEX3) PCA module 3 input/PWM output. P4.4(/SS) SPI Slave Select output. P4.5(SCK) Serial Clock of SPI controller. P4.6(MISO) Master Input Slave Output of SPI controller. P4.7(MOSI) Master Output Slave Input of SPI controller.
ECI	I L	PCA external clock input
CP0+ CP0- CP1+ CP1-	A I	CP0+ Comparator 0 Non-Inverting Input. CP0- Comparator 0 Inverting Input. CP1+ Comparator 1 Non-Inverting Input. CP1- Comparator 1 Inverting Input.
DAC0 DAC1	A O	DAC0 DAC 0 Voltage Output. DAC1 DAC 1 Voltage Output.

Note: Type I: input, O: output, I/O: bi-directional, S: Schmitt trigger input, H: pull-high, L: pull-low, A: analog

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